Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **V 1+**

**3 IN A**

**4 IN B**

**6 V 1-**

**8 STROBE B**

**9 OUT B**

**10 GND**

**11 OUT A**

**13 STROBE A**

**14 V 2+**

**3 4 6**

**13 11 10**

**9**

**14**

**1**

**8**

**49 mils**

**39 mils**

**MASK**

**REF**

**4002A**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 4002A**

**APPROVED BY: DK DIE SIZE .039” X .049” DATE: 3/3/16**

**MFG: SIGNETICS THICKNESS .021” P/N: NE529**

**DG 10.1.2**

#### Rev B, 7/19/02